low energy, to form a surface-implantation layer **24** in the proximity of the top surface **3***a* of the epitaxial layer **3**. The implantation is made prior to the formation of the columnar structures **7** and, for example, after the formation of the first doped region **4** and of the ring region **5** in the edge area **1***b*. It should be noted that, in this case, the first doped region **4** does not extend in the active area and comprises only the edge portion **4***b*.

[0039] The process proceeds with the steps described previously in

[0040] FIGS. **4** to **6**, concerning the edge-termination structure, namely, with formation of the columnar structures **7**, etching of the wrinkled surface layer **9** in the edge area **1***b* and consequent definition of the step **13**, and formation of the field-oxide layer **15**.

[0041] Next (FIG. **14***b*, showing an enlarged portion of the active area, to which the subsequent process steps refer), in a surface region of the connection portions **11**, between adjacent surface extensions **10** of the columnar structures **7**, N-type implantations are carried out to form surface contact regions **25**.

[0042] This is followed (FIG. **14***c*) by a thermal diffusion process for definition of sinkers **26** of an N type, which reverse the conductivity of the respective connection portions **11** and reach the underlying surface-implantation layer **24**, also of an N type. On the wafer, once again limitedly to the active area, a gate-oxide layer **27** is then grown, on top of which a polysilicon layer is deposited and subsequently etched so as to obtain gate regions **28** at the top of the sinkers **26**.

[0043] Next (FIG. **14***d*), a P-type body implantation is carried out, through the gate-oxide layer **27** and exploiting the gate regions **28** as "hard mask", which is followed by a thermal diffusion process, to form body regions **29**. The latter extend inside the surface extensions **10** of the columnar structures **7**, consequently reproducing the non-planar profile thereof with grooved cross section, and partially inside the sinkers **26** beneath the gate regions **28** (where they form channel regions of the transistor).

[0044] A P^{++}-type deep-body implantation is then carried out (FIG. **14***e*), having, for example, the same characteristics (in terms of energy and dose) as those of the implantation leading to formation of the first doped region **4**. This is followed by a thermal diffusion process to form deep-body regions **30** in a central area of the surface extensions **10**. Next, a N^+-type source implantation is carried out to form source regions **32** inside the body regions **29** and deep-body regions **30**. This is followed by a process of deposition and definition of a dielectric layer to form insulating regions **33** on the gate regions **28**, and opening of contacts. At the end of the manufacturing process, a power MOS transistor is consequently obtained on a non-planar surface, with a gate oxide and gate region in a planar area and a body region in a non-planar area (in particular made inside the surface extension of a charge-balance columnar structure).

[0045] FIG. **14***f* shows the final structure of the MOSFET with the corresponding edge structure, obtained with final steps of formation of the second doped region **18** for the cathode contact, of metallization, and of passivation, in a way similar to what has been described previously. In particular, the deep-body region **30** of the last active cell (or stripe) of the transistor is connected to the edge portion **4***b* of the first doped region **4** (anode of the diode of the edge termination).

[0046] A second variant of the manufacturing process of a charge-balance MOSFET initially envisages the process steps described with reference to FIGS. **3** to **6** concerning the edge-termination structure, namely, with formation of the edge portion **4***b* of the first doped region **4** (which once again does not extend into the active area) and of the ring region **5**; formation of the columnar structures **7**; etching of the wrinkled surface layer **9** in the edge area **1***b* and consequent definition of the step **13**; and formation of the field-oxide layer **15**.

[0047] In the active area, a P-type surface implantation is then performed to form a body layer **35** (FIG. **15***a*), which extends within a surface portion of the wrinkled surface layer **9**. Next, an N-type blanket implantation is performed on the surface of the wafer **1** (once again in the active area), to form a source layer **36**, which is located in a surface portion of the body layer **35**.

[0048] A deep implantation is then carried out to form deep-body regions, designated once again by **30**, at the surface extensions of first columnar structures, and not in second columnar structures that alternate to the first columnar structures inside the epitaxial layer **3** (FIG. **15***b*). Next, in the connection portions **11** of the wrinkled surface layer **9** surface trenches **37** are opened, which traverse the connection portions **11** and reach the underlying epitaxial layer **3**. The surface trenches **37** define body regions **29** of the transistor.

[0049] In the active area, a gate-oxide layer **38** is then grown on the wafer **1** (FIG. **15***c*), deposited on top of which is a polysilicon layer **39**, of a conformable type, which fills the surface trenches **37**.

[0050] The polysilicon layer is then etched so as to obtain gate regions **28** in areas corresponding to the surface trenches **37** (FIG. **15***d*). This is followed by a process of deposition of a dielectric layer to form insulating regions **33** on the gate regions **28**, and opening of the contacts. At the end of the manufacturing process a power MOSFET is consequently obtained on a non-planar surface, with oxide and channel regions in an area defined by a trench-formation process. In particular, the channel region extends vertically inside the body layer **35** between the source layer **36** and the epitaxial layer **3**, at the sides of the surface trenches **37**. The body region is in a non-planar area, inside the surface extension of a charge-balance columnar structure.

[0051] Shown in FIG. **15***e* is the final structure of the MOSFET with the corresponding edge structure, made with final steps of formation of the second doped region **18** for the cathode contact, metallization, and passivation, in a way similar to what has been described previously. In particular, the body region **29** of the last active cell (or stripe) of the transistor is connected to the edge portion **4***b* of the edge-termination structure.

[0052] Advantages of the described manufacturing process and of the resulting structures are clear from the foregoing description.

[0053] First, the process enables a charge-balance power diode and a corresponding efficient edge-termination structure to be obtained, which enables maximization of the performance in reverse biasing of the device.

[0054] The edge-termination structure can be easily integrated in power devices (for example, MOSFETs) based upon the charge-balance concept. In particular, the process described envisages removal in the edge area of the wrinkled surface layer that is formed after the formation of the charge-balance columnar structures, and the etching for this removal